

Abstract of the Disclosure

The present invention relates to a method for fabricating semiconductor device with negative differential conductance or transconductance. According to the present invention, a fabrication process thereof can be simplified by using an SOI (Silicon-On-Insulator) substrate, and a tunneling device exhibiting the negative differential conductance or transconductance at room temperature can be implemented by using P⁺-N⁺ junction barriers as tunneling barriers and implanting impurity ions into a channel region so that their density is higher than the effective density of states where electrons or holes can exist thereon. Since the semiconductor device with the negative differential conductance or transconductance can be also be implemented even at room temperature, there is an advantage in that the present invention can be applied to an SRAM or a logic device using a device which can be turned on/off in response to a specific voltage.

Further, according to the fabrication method of the present invention, miniaturization of the device can be easily made, and the reproducibility and the mass productivity of the process can be enhanced. Simultaneously, the gate, the source/drain and the channel regions are formed by the self-aligned process. Thus, there is another advantage in that a gate pitch can also be reduced.

In addition, there is a further advantage in that the semiconductor device fabricated according to the present invention has the characteristic of a single electron transistor by using the channel region as the quantum dot and the two P⁺-N⁺ junctions as the tunneling barriers.